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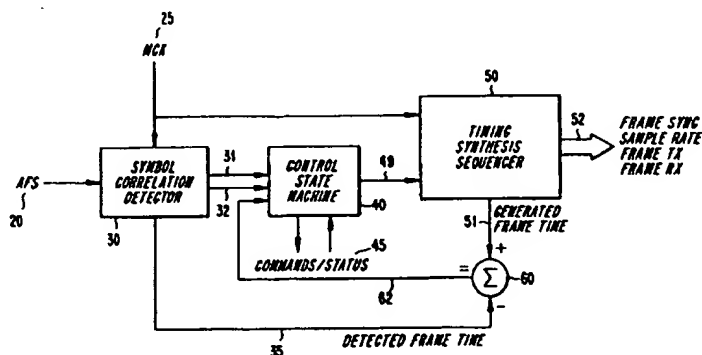
(57) **Abstract**

A distribution reference signal is described for use in synchronizing data transmission. The distribution reference signal includes a digital symbol pulse train having a rate much higher than the actual reference frequency represented. A fixed group of symbols is used to identify a low frequency signal event or reference pulse. A second group of sequence symbols indicates continuous phase information. The symbols used to identify the reference pulse are significantly different from the other phase information facilitating identification of the reference pulse. By encoding a known sequence of symbols to represent the phase information in the reference signal, an increased amount of frequency information can be propagated as compared with a single pulse aiding the detection and correction of signalling errors as the errors will break the expected symbol sequence. A system can then identify and correct or choose to ignore the errors based on the effect the errors will have on the system performance.

-1-

ERROR CORRECTING TIMING REFERENCE DISTRIBUTION

BACKGROUND

The present invention relates generally to global time reference signals

5   for use in telecommunications systems and more specifically for airframe
synchronization.

Synchronization is an important part of many telecommunications
systems. In order to provide system synchronization, a communications system needs
to distribute accurate frequency and time reference signals. For example, in a time

10   division multiple access (TDMA) mobile communications network, a base station
transmits bursts of data known as airframes (or simply frames), to mobile units
traveling in an area serviced by the base station. In an American Digital Cellular
(ADC) system for example, a frame is defined as a digital packet containing six time
slots transmitted at a 25 Hertz frame rate. This exemplary frame format, illustrated

15   as FIG. 1, is used in the D-AMPS system specified in EIA/TIA IS-54B. However,
those skilled in the art will appreciate that other systems, such as that specified by
Global System for Mobile Communication (GSM), may provide different frame/time
slot formats and timing.

Consider the situation depicted in FIG. 2. An original base station BS1

20   is handling a connection between mobile station MS and the network as represented
by the transmission link TL1 between base station BS1 and the mobile switching
center MSC. The mobile station then moves to a position MS' wherein it is
determined that this connection is best handled by base station BS2, e.g., to improve
the signal quality of the connection. The system initiates a handoff procedure by

25   sending appropriate commands to base stations BS1 and BS2 over transmission links
TL1 and TL2. The mobile station MS may or may not be informed of the impending
handoff.

At some time after the handoff decision is made, transmissions will
begin from the base station BS2 and terminate from base station BS1. In some cases,

30   e.g., where a mobile station has the capability of performing diversity combination or
selection of plural signals, it may be desirable to allow transmission to continue from

-2-

both base stations for some time period. In other cases, it may be desirable to have little or no overlap in the transmissions from base stations BS1 and BS2. In either scenario, it is important to ensure that no frames are lost during the handoff procedure. Thus, it is desirable that the mobile station cleanly receive a last frame

5   from original base station BS1 followed by a first frame from base station BS2. This involves at least two timing aspects: (1) estimating the difference in propagation delay between the original base station BS1 and the mobile station MS and that between the new base station BS2 and the mobile and (2) synchronizing the transmissions between the base stations so that the frames from each base station arrive at the mobile station

10   at the desired times.

Providing such synchronization however is difficult as there is very little gap time between the transmitted frames. In order to synchronize the transmission of the frames of the two different base stations, BS1 and BS2, a highly accurate and quickly discernible reference signal must be provided such that the base stations are time

15   synchronized within, for example, 2 microseconds to ensure that the frame decoder in the mobile will not be disturbed by lost, or duplicated data.

A second application for the synchronization of airframes in a telecommunications system occurs when a single base station contains multiple transceivers that are each transmitting the same, or substantially the same, information

20   to a mobile unit. The transceivers can be separated within the same base station or base station site, or transceivers from neighboring sites can cooperate for a call handled by a common switching center, wherein the neighboring sites are globally synchronized. Each transceiver can transmit at slightly different frequencies in order to avoid interference. As the base station transmits the airframes to a mobile unit, the

25   mobile unit receives each of the signals and combines them such that the signals appear much stronger. This is often referred to as simulcasting. One way to achieve a working simulcasting is to synchronize the airframe timing of two transceivers and then have the transceivers transmit airframes with a known offset relative to each other. However, in order to be able to combine the signals when received at the

30   mobile station, the transmission of signals must be synchronized by the base stations. For this application, synchronization between transmitters should be determined

within, for example, ten microseconds. In order to synchronize the airframes, airframe data clocks and synchronization signals are phase locked using a reference distribution signal.

In any communications system, accurate distribution of frequency and time reference signals is complicated and expensive. The distribution of timing reference signals is also a continuous source of errors that can be difficult to determine. To provide synchronization in a communications system, a phase-locked loop (PLL) can be used to lock to a reference frequency. For example, a typical analog PLL may include a phase comparator, a low-pass filter and a voltage controlled oscillator (VCO). According to this arrangement, the output of the VCO is fed back as one of the inputs to the phase comparator and, typically, a low frequency reference signal consisting of individual synchronization pulses is fed into another input of the phase comparator. As a result of this configuration, the receiver will be very susceptible to errors picked up in the timing reference signal distribution medium. For example, in conventional systems, when spurious frequency deviations of the reference signal cause errors, these errors are propagated through the feedback loop. This in turn may move the VCO out of its specified operating frequency range, resulting in a breakdown of communications. In addition, these errors can also add to the initial time required to obtain locked condition. This in turn prevents conventional systems from obtaining the synchronization accuracy needed for the applications described above. Unfortunately detection and correction of spurious or deviating timing pulses is very difficult in these conventional systems.

It is therefore an object of this invention to distribute a timing reference signal that is less sensitive to errors and which will minimize the propagation of errors.

Another object is to enable the transceiver to obtain a phase-locked state with respect to the reference signal significantly faster than is presently possible with conventional systems and that will maintain a lock even if spurious errors or interference are introduced in the reference signal.

It is a further object to make fault identification of the distributed reference signal easier, so that the reference receiver will obtain accurate alarms

-4-

concerning cable shorts, cable open circuit, and spurious signalling. In addition, it is an object of the invention to provide a reference signal distribution while minimizing manufacturing costs of the communications system.

5   **SUMMARY**

The foregoing and other objects are accomplished according to exemplary embodiments by distributing a reference signal that includes an encoded digital symbol pulse train having a rate much higher than the actual frequency or occurrence rate of a reference event represented (For example a frame time zero that

10   occurs once every 40ms frame for a 25Hz signal). A first group or sequence of symbols is used to identify a low frequency signal event or reference event. A second group or sequence of symbols is used to indicate continuous phase information. The symbols used to identify the reference event are made significantly different from the phase information, making identification of the reference event easier. By encoding a

15   known sequence of symbols to represent the phase information in the reference signal, an increased amount of frequency information can be propagated as compared with a conventional single pulse. This also facilitates the detection and correction of signalling errors as the errors will break the expected symbol sequence. The system can then identify and correct, or choose to ignore, the errors based on the effect the

20   errors will have on system performance.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the invention will be understood by reading the following description in conjunction with the drawings, in which:

25   FIG. 1 illustrates a frame with time slots;

FIG. 2 shows an example of base station communication with a mobile;

FIG. 3A illustrates phase relations of the timing reference signal;

FIG. 3B shows the timing reference signal in relation to an indicated frame time zero;

30   FIG. 4 is a block diagram of a digital phase locked loop;

FIG. 5 is a block diagram of an exemplary symbol correlation detector;

-5-

FIG. 6 depicts sampling and bit error correction according to an exemplary embodiment of the present invention;

FIG. 7 is a block diagram illustrating an exemplary embodiment of a symbol detection unit; and

FIG. 8 is a block diagram of transceiver cabinets to which reference signals according to the present invention can be distributed.

DETAILED DESCRIPTION

The various features of the invention will now be described with respect to the figures, in which like parts are identified with the same reference characters.

AIRFRAME REFERENCE SIGNALS

The distribution of accurate frequency and time reference signals in telecommunications systems can be complicated and expensive. Reference signal distribution is a source of continuous errors that are difficult to detect and locate. Errors can also lead to severe degradation of system performance. The technique and medium used to distribute a reference signal, *e.g.*, as microwave, radio, or cable, introduce spurious pulses or errors in the signal which, if undetected, can slow or inhibit system operation. For example, when a conventional reference signal is received in a phase locked loop (PLL), the error in the reference signal is added to the feedback loop, causing the system to take much longer to acquire a locked frequency. As a result, the PLL could be forced outside the maximum specified error from the ideal reference frequency for the system.

The problem with conventional reference signals is that it is extremely difficult to determine if errors or unwanted interference have been added to the reference signal. It is equally difficult to remove any errors that have been introduced in the reference signal.

According to one aspect of the present invention, a time domain discrete reference signal is distributed and encoded with information to enable the system to determine if the reference signal has enough accuracy. The reference signal

-6-

includes predetermined groups or sequences of symbols. By monitoring the reference signal the system can determine if each received sequence of symbols is correct for the actual frequency measurement. If the sequence is not correct, the system can then determine if the signal should be disregarded. The system can thus exclude a very

5   small part of the reference signal that contains an error. Therefore, a much higher level of disturbance or noise is needed to break a lock condition. The symbols are chosen so that, for example, spikes, cable breakage, hum, click, and static will not appear as a good signal. The system is then able to pick system errors out of the reference system errors and make corrections on single samples to make the reference

10   signal immune to small spikes and jitter that equals out on a single symbol or in an alternative embodiment simply ignore the error. For example, errors smaller than plus or minus 1.5 master clock (MCK) intervals will be filtered by sampling and symbol detection units (shown in detail below) under the condition that the error will be equaled by an error of the same amount in the other direction at the next transition

15   on the reference signal.

The rate of symbol transmission is also important to the ability to disregard spurious errors. As the system has to regard the period of a symbol error(s) in comparison to the measurement interval, a symbol error with a period of 1/1000 of a measurement interval will render in the reference signal an error of one

20   per mille or 1/1000. Therefore, the smaller the symbol period, the higher the symbol transmission rate and correspondingly the greater the ability to disregard errors. A conventional PLL system with one pulse per reference event will respond to a single spike as anything between zero error up to the whole pulse interval. When using such a conventional reference signal only a single spike per (theoretically) eleven hours is

25   tolerated; however, when implemented with a PLL including a lowpass filter present in the feedback chain, about a single spike per hour can be tolerated. By using the airframe reference signal for synchronization according to the present invention, the initial time needed to produce a locked condition will be much smaller than with a conventional reference signal. Another advantage of using a known sequence of

30   symbols is the ability to count errors and determine the reliability of the reference signal. For the same reasons the system can also recognize errors much more quickly

-7-

and disregard or hold the signal locked within the required specification by keeping errors from being fed back into the PLL. As a result, fewer demands are placed on the circuitry.

According to another embodiment of the invention, more phase
5   information is sent with the reference signal than is actually needed to indicate a reference event. In order to diversify the information, the phase information must behave in a way that is sufficiently different from the reference event such that the reference event is easily identified. The information is comprised of symbols each having a unique bit pattern. There are basically two kinds of symbols, "phase"
10 symbols and "sync" symbols. The sync symbols carry both the reference event and phase information. The phase symbols only carry phase information. Symbols are indicated by a continuous flow of a unique high frequency pattern. According to one embodiment of the invention, the symbol pattern is one million times more unique than the singular pulse used in a conventional system. This will satisfy one parts per
15 million (PPM) of information consistency simplifying the detection of any error condition and if an error condition can be corrected.

Turning to FIG. 3A, an airframe timing reference (AFS) signal is shown. The AFS signal is a composite signal comprising two binary signals, AFS1 10 and AFS2 11. According to a preferred embodiment of the invention, the AFS
20 signal can be generated out of a 4860 kHz clock signal, CLK 12. Therefore, for a 25 Hz reference pulse, with every 48,600th tick of CLK, a violation sequence 14 is indicated. The violation sequence is a sequence of sync symbols recurring in the stream of symbols at the time of the reference event. According to one preferred embodiment of the invention the violation sequence occurs at a 25 Hertz rate. The
25 violation sequence lasts for two cycles of the CLK 12, starting at the negative CLK transition. After completion of the violation sequence, the normal sequence composed of phase symbols 15 is resumed and will continue until the next violation sequence, completing a 25 Hertz cycle.

FIG. 3A illustrates that the order of the toggle between AFS1 10 and
30 AFS2 11 is reversed during the violation sequence. For example, in FIG. 3A AFS1 10 would normally remain low and AFS2 11 would toggle low. However, with the

-8-

beginning of the violation mask AFS2 11 is held high and AFS1 10 toggles high. In other words, with the beginning of a violation sequence, AFS2 11 will toggle when AFS1 10 normally would have toggled, and vice versa. Through use of the chosen encoding scheme, the AFS signal will propagate an airframe time reference (airframe

5   timing) with high tolerance to disturbances and connection errors for several reasons. First, the frequency of symbols is very high. This makes singular errors very insignificant. Second, there are more symbols that can be represented than actually are used. Therefore an error will likely generate a symbol that is not accepted. However, even in the unlikely event the error signal mimics one of the allowable

10   symbols, it will not appear in the correct or expected sequence and thus also be identifiable. In addition, if AFS1 and AFS2 toggle at the same time, an illegal symbol will be generated.

Frame time zero, FTZ 16, is indicated by the violation sequence as shown in FIG. 3A. The Detected AFS and FTZ can be determined in many ways.

15   According to a preferred embodiment, FTZ and the Detected AFS are determined when all of the sync symbols have been received with no errors and in the right sequence. If any of the sync symbols are faulty, the whole 40 ms interval is disregarded. Using this embodiment it has been discovered that phase information is not necessary for the determination. It is enough to just count the phase information

20   errors in order to determine the signal jitter, and other errors. It will be appreciated by one skilled in the art that the signals in FIG. 3A, except for AFS1 and AFS2 are included only for illustrative purposes of determining a reference event and are not part of the AFS distribution concept per se. Other signaling schemes for creation of a reference signal would suggest themselves to one skilled in the art without departing

25   from the scope and spirit of the invention.

According to a preferred embodiment of the invention, the airframe timing reference signal, AFS, can be a 1215 kHz, 50/50% duty-cycle 90° two phase square-wave signal carried by the signals AFS1 and AFS2. The 25 Hz interval airframe timing is encoded into the AFS signal by means of a phase violation as

30   defined above. The coding scheme used is similar to a two-phase Miller variant or delay modulation encoding. Of course other coding schemes may be used in

accordance with the present invention. According to this embodiment, jitter on the AFS signal must not exceed ± 25 nanoseconds at the receiver end. Also according to this exemplary embodiment, the maximum allowed frequency error on the AFS signal is 1 PPM measured over an integration time of 25 milliseconds, or longer. These

5   values have been chosen because they do not limit design of a system and are loose when compared with actual system performance. A path delay introduced by distributing the AFS signal from the timing master and to any airframe time reference recipient is allowed to be between 0 - 450 nanoseconds. Also according to the preferred embodiment of the invention a Master Clock of 19.44 MHz is used. As

10   indicated in FIG 3B, one AFS minimum transition interval TM 17 4.86 MHz, which is approximately 206 nanoseconds; TC equals 4.86 MHz divided by 4 = 1215 kHz, or approximately 823 nanoseconds.

SYMBOL DETECTION AND CORRELATION

15   The airframe timing is presented on the incoming time reference signal, AFS, as a train of symbols, see, e.g., FIGS. 3A and 3B. Each symbol represents a specific time in the airframe. As previously mentioned, the time reference signal is diversified into AFS1 and AFS2. Each of the two signals carries a part of the composite AFS signal. In order to simplify the following description, the two signals,

20   AFS1 and AFS2, will be commonly referred to as AFS, and where they differ, this will be noted.

             In order to generate the airframe timing signals 52, see, e.g., FRAMESYNC, SAMPLERATE, FRAME_TX, and FRAME_RX in FIG. 4, they may be synchronized to a timing reference signal. Once an AFS signal is generated

25   the signal can be decoded by the receiving unit (see, e.g., FIG. 8), for instance a transceiver in the base station. The receiving unit identifies and correlates the phase information and the reference event information or SYNC information. According to another aspect of the present invention this can be accomplished through the use of a symbol correlation detector (SCD).

30   The SCD detects airframe timing on the AFS signal by measuring the time between the current transition on the incoming reference and the last transition

-10-

on AFS1 and AFS2, respectively. It also measures the current signal level and detects transitions on the AFS1 and AFS2. FIG. 5 is an example of an SCD 30 according to an exemplary embodiment of the invention. The AFS signal 20 and master clock (MCK) 25 are fed into a sampling and bit error correction unit 34.

5   After the AFS signal is sampled and corrected, it is output as a detected AFS (DET_AFS) signal 37. The DET_AFS 37 is then input into a symbol detection unit 36 to identify the symbols in the AFS signal to determine the encoded reference event information and phase information which is outputted as signals AFS_TRANS 39 and SYMBOL ID 33. These signals are then input into the Frametime Detection Unit 38

10   along with the detected AFS signal 37 in order to identify any symbol error, overrun, and the detected frame time 31, 32 and 35, respectively.

SAMPLING AND BIT ERROR CORRECTION

       One advantage of using a discrete reference signal is the ability to

15   identify errors and deviations that can occur with distribution of the reference signal. Turning to FIG. 6, an exemplary implementation of sampling and bit error correction unit 34 is depicted. The AFS signal is input into a low pass filter 41 and then transmitted to a Schmitt trigger 42. The signal is then sampled in a series of D-type latches 43. Single bit errors are then corrected using a two out of three majority gate

20   44. The sampled and corrected signal, DET_AFS 37 is then distributed to the symbol detector. It should be noted that this function is doubled, one for AFS1 and one for AFS2.

SYMBOL DETECTION AND ERROR IDENTIFICATION

25   FIG. 7 shows an example of a symbol detection unit 36 according to an embodiment of the invention. The symbol detection unit 36 detects transitions on the detected AFS signal 37. Time between the transitions is measured with a 5-bit counter 55 that counts from three after it is reset by the AFS_TRANS asserted condition 39. The detected AFS signal 37 is "mid bit sampled" as the AFS signal is

30   nonstationary to the sampling MCK signal. Since the count by the counter 55 is truncated, and counts the duration of a level sampled at mid bit, the counter should

-11-

start at three to compensate for the truncated bit. The counter counts up to 16 and then holds until reset again. The detected SYMBOL ID 33 equals the binary output of the counter 55 divided by 4. According to a preferred embodiment of the invention, Symbol IDs from the symbol detector are as follows: 0 = burst error; 1 = symbol 1; 2 = symbol 2; 3 = symbol 3; and 4 = overrun error. Note this function is doubled, one for AFS1 and one for AFS2.

Frame time is detected by comparing the states of DET_AFS1/DET_AFS2, AFS_TRANS1/AFS_TRANS2, and SYMBOL_ID1/SYMBOL_ID2. Table I depicts an example of valid symbols which can be used according to the teachings of this invention:

<div align="center">

TABLE I

DET_AFS 1	2	AFS_TRANS 1	2	SYMBOL_ID 1	2	Condition
1	1	1	0	1	2	SYNC (-1)
1	0	0	1	1	3	SYNC (0)
0	0	1	0	2	1	SYNC (+1)
0	1	0	1	1	2	SYNC (+2)
0	0	0	1	2	1	SYNC (+3)
1	0	1	0	3	1	SYNC (+4)
1	0	1	0	2	1	Phase (0)
1	1	0	1	1	2	Phase (1)
0	1	1	0	2	1	Phase (2)
0	0	0	1	1	2	Phase (3)
X	X	X	X	4	X	OverRun
X	X	X	X	X	4	OverRun

</div>

Symbols are detected at any transition on AFS_TRANS1 and AFS_TRANS2. An exception to this, occurs with an OverRun error, which is detected every master clock interval that the situation remains. OverRun error is flagged when there are no transition on one of the two or both of the signals AFS1 and AFS2 for a timeout period. According to one preferred embodiment the timeout period is approximately 211 microseconds (4096x51.44=210698, where 4096 is an up/down counter value, and time quantum 51.44ns=1000 divided by the master clock or 19.44). The timeout is sampled with an up/down counter (not shown) that counts

-12-

overruns per MCK interval. The counter will count down to zero and stay there if
there are no overruns. The counter will count for each overrun up to 8191. An
overrun error can occur when connection is broken, *e.g.*, cable breakage, when no
signal is detected. An overrun error is flagged when this counter is greater than or
equal to 4096. The OverRun error thus is filtered for glitches and reported as a
SymOverRun when it averages more than 50% over an integration time of 211
microseconds. When the condition from the above Table I is SYNC(0), frame time
zero (FTZ) is detected. Continuous indication of momentary phase is given by the
phase (n) symbols. The detector keeps track of the sequence by validating the
detected condition according to the previous condition.

Table II indicates an example of a series of valid condition sequences.
Note this table is exemplary and other encoding schemes could be used without
departing from the scope and spirit of the invention.

TABLE II

Previous:	Current:
Phase(0) =>	Phase(1)
Phase(1) =>	Phase(2)
Phase(2) =>	Phase(3)
Phase(3) =>	Phase(0)
Phase(2) =>	Sync(-1)
Sync(-1) =>	Sync(0)
Sync(0) =>	Sync(1)
Sync(1) =>	Sync(2)
Sync(2) =>	Sync(3)
Sync(3) =>	Sync(4)
Sync(4) =>	Phase(1)
overrun =>	Any condition
symerror =>	Any condition

A detected condition that is out of sequence is considered as a symbol
error. For instance, if the previous symbol was Phase(1) the expected current symbol
should be Phase(2). If not then an error is detected. When any error condition
occurs, the detected frame timing is not considered valid and a symbol error is
reported at every transition on either DET_AFS1 or DET_AFS2. Conditions of

-13-

symbol error, and implicitly overrun errors, too, will not affect the generated frame timing. Therefore, the detected frame timing can be updated frequently. The system can also count the number of errors to determine if the signal has become unlocked. The system can then decide if it should adjust the loop back time in the phase locked

5   loop or if the system can go temporarily unsynced if the error is spurious.

FREQUENCY GENERATOR AND CORRELATOR

One application of the timing reference signal is to provide airframe synchronization between base stations and between local transceivers at the same base

10   station as illustrated in FIG. 8. According to this embodiment a time reference signal EXT_AFS 72 is generated by a timing master TIM (not shown). The EXT_AFS is then distributed between the transceiver cabinets 70. The EXT_AFS is then distributed internally to each transceiver 80 as signal AFS 82. Each transceiver 80 then locks its airframe timing to this time reference signal.

15   The synchronization can be accomplished through use of a Frequency Generator and Correlator (FGC) or discrete phase locked loop as shown by FIG. 4. Each transceiver 80 is provided with an FGC. In order to synchronize the transmissions of the airframes from each of the base stations and from multiple transceivers within a base station, a timing reference signal (AFS) 20 is provided.

20   The FGC generate airframe timing signals using the MCK 25. In order to maintain synchronization to AFS signal 20, the FGC adds or removes a small time quantum at regular intervals to the airframe timing signals 52.

In an ideal situation of no time skew between the generated timing and the AFS reference signal, the FGC generates its output signals directly out of the

25   MCK. When a time skew between the generated timing and the reference AFS signal is present, the FGC will adjust timing by adding or removing a quantum of time to or from the generated airframe timing signals. This time quantum is determined by the Timing Synthesis Sequencer and is proportional to the MCK.

By regularly skewing the generated timing signals in the FGC, the

30   signals become phase locked to the AFS signal. A complete description of the FGC and its operation is given in co-pending U.S. Application No. 08/_____,

-14-

Attorney Docket No. 027555-482, titled "Discrete Phased Locked Loop" by Johan Jansson, filed on the same date and incorporated herein by reference.

The present invention has been described by way of example, and modifications and variations of the exemplary embodiments will suggest themselves to
5   skilled artisans in this field without departing from the spirit of the invention. The preferred embodiments are merely illustrative and should not be considered restrictive in any way. The scope of the invention is to be measured by the appended claims, rather than the preceding description, and all variations and equivalents which fall within the range of the claims are intended to be embraced therein.

-15-

WHAT IS CLAIMED IS:

1.   A system for distributing a timing reference signal comprising:

          means for generating a timing reference signal, wherein the timing

5   reference signal includes a group of symbols each representing a specific time;

          means for distributing a timing reference signal to at least one of a

plurality of units; and

          means for detecting and correlating the timing reference signal at the at

least one of the plurality of units.

10

2.   The system according to claim 1 wherein the detection means further

comprises a sampling and bit error correction unit for determining bit errors in the

timing reference signal.

15   3.   The system according to claim 1 wherein the detection means further

comprises a symbol detection unit for identifying the symbols in the timing reference

signal and determining a sequence of symbols.

4.   The system according to claim 3 wherein the symbol detection unit

20   determines if the sequence of symbols differs from a predetermined sequence of

symbols.

5.   The system according to claim 4 wherein the symbol detection unit

stores the number of deviations from the predetermined sequence of symbols.

25

6.   The system according to claim 1 wherein the timing reference signal

symbols are either SYNC symbols or PHASE symbols wherein a SYNC symbol

indicates a reference EVENT and phase information and a PHASE symbol indicates
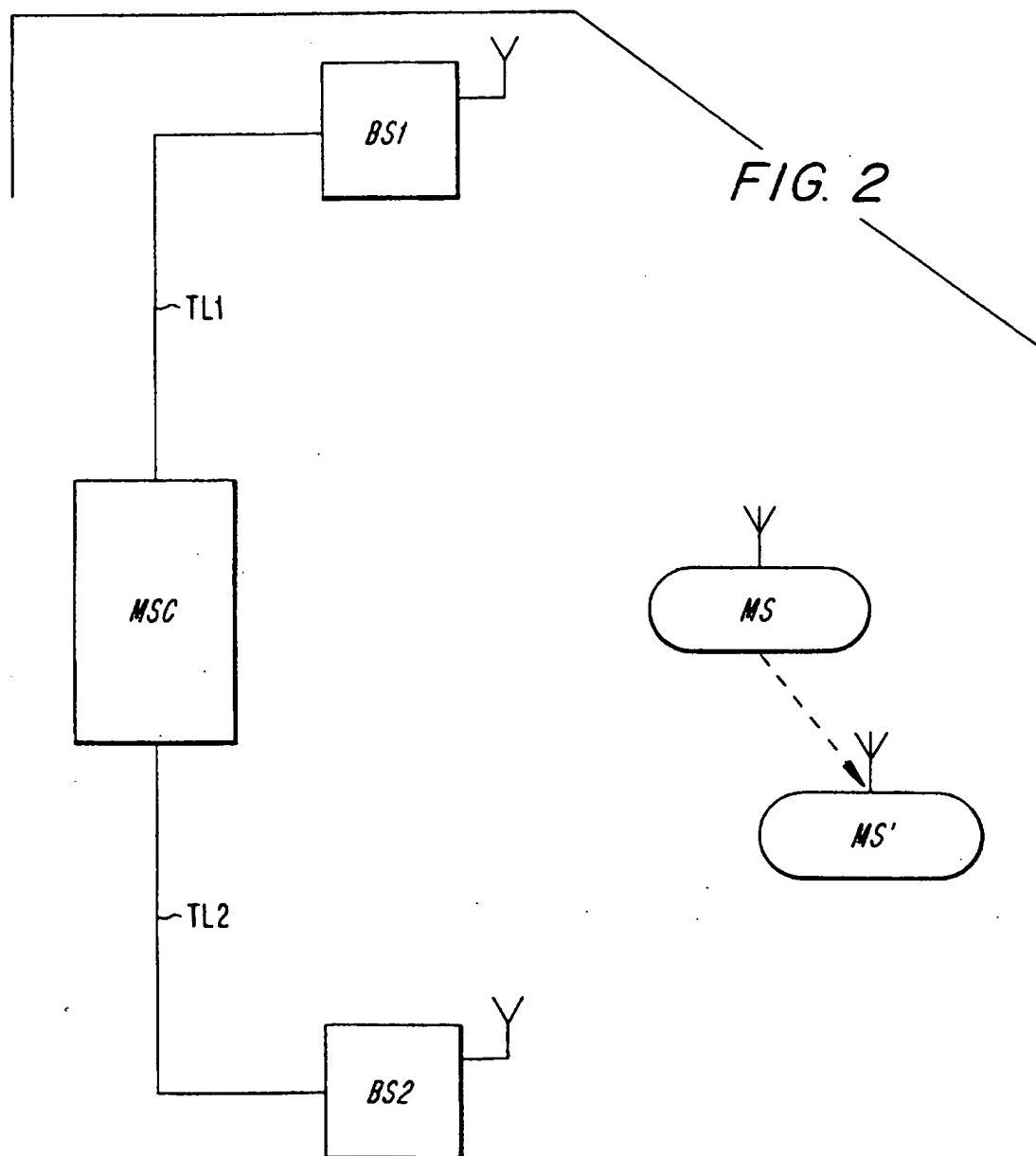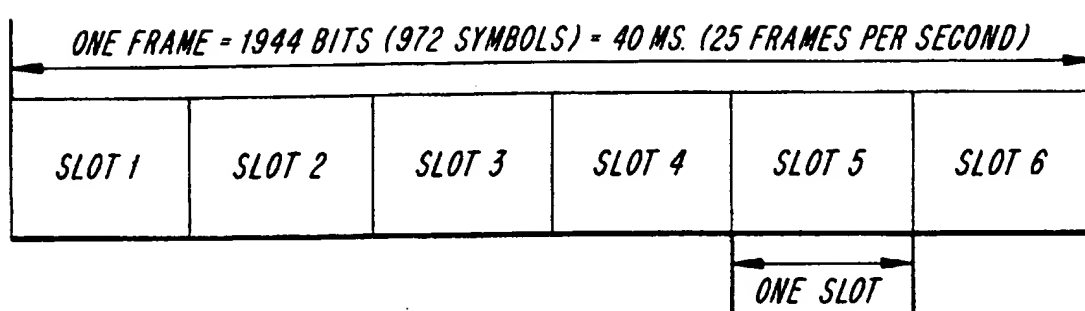
phase information only.

30

-16-

7.   The system according to claim 6 wherein the SYNC symbols are low frequency events and PHASE symbols are high frequency events.

8.   The system according to claim 6 wherein the group of symbols are
5   transmitted according to a predetermined sequence.

9.   The system according to claim 6 wherein the timing reference signal is a composite of at least two discrete signals.

10   10.   The system according to claim 1 wherein the means for detecting and correlating includes a discrete phase locked loop.

11.   A method for distributing a reference timing signal in a telecommunications system comprising the steps of:
15   generating a timing reference signal containing oversampled reference timing information; and
                distributing the timing signal to a plurality of units.

12.   The method according to claim 11 further comprising the steps of:
20   detecting and correlating the timing reference signal in at least one of the plurality of units;
                generating at least one data frame synchronization signal from the detected and correlated signal; and
                synchronizing data frames in at least one of the plurality of units using
25   said data frame synchronization signal.

13.   The method according to claim 11 wherein the reference timing signal comprises a fixed sequence of symbols indicating reference EVENTS and continuous phase information.

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-17-

14.   The method according to claim 12 wherein the reference EVENTS are low frequency events and the continuous phase information is a high frequency event.

15.   The method according to claim 11 wherein the timing reference signal
5   is a composite of at least two discrete signals.

16.   The method according to claim 15 wherein the step of generating a timing reference signal further comprises:

          generating a violation sequence for interrupting phase symbols to
10   indicate a reference EVENT; and

          ending the violation sequence to resume PHASE symbol transmission.

17.   The method according to claim 16 wherein the violation sequence is generated in a 25 Hz cycle.
15

18.   The method according to claim 12 wherein the step of detecting further comprises detecting errors in the timing reference signal.

19.   A discrete timing reference signal for synchronizing data frame
20   transmission, comprising:

          discrete SYNC SYMBOL indicating reference events and phase information;

          discrete phase symbols indicating continuous phase information only;

          wherein the symbols are ordered in a predetermined fixed sequence and
25   wherein the SYNC symbols are a low frequency event and the phase symbols are high frequency events.
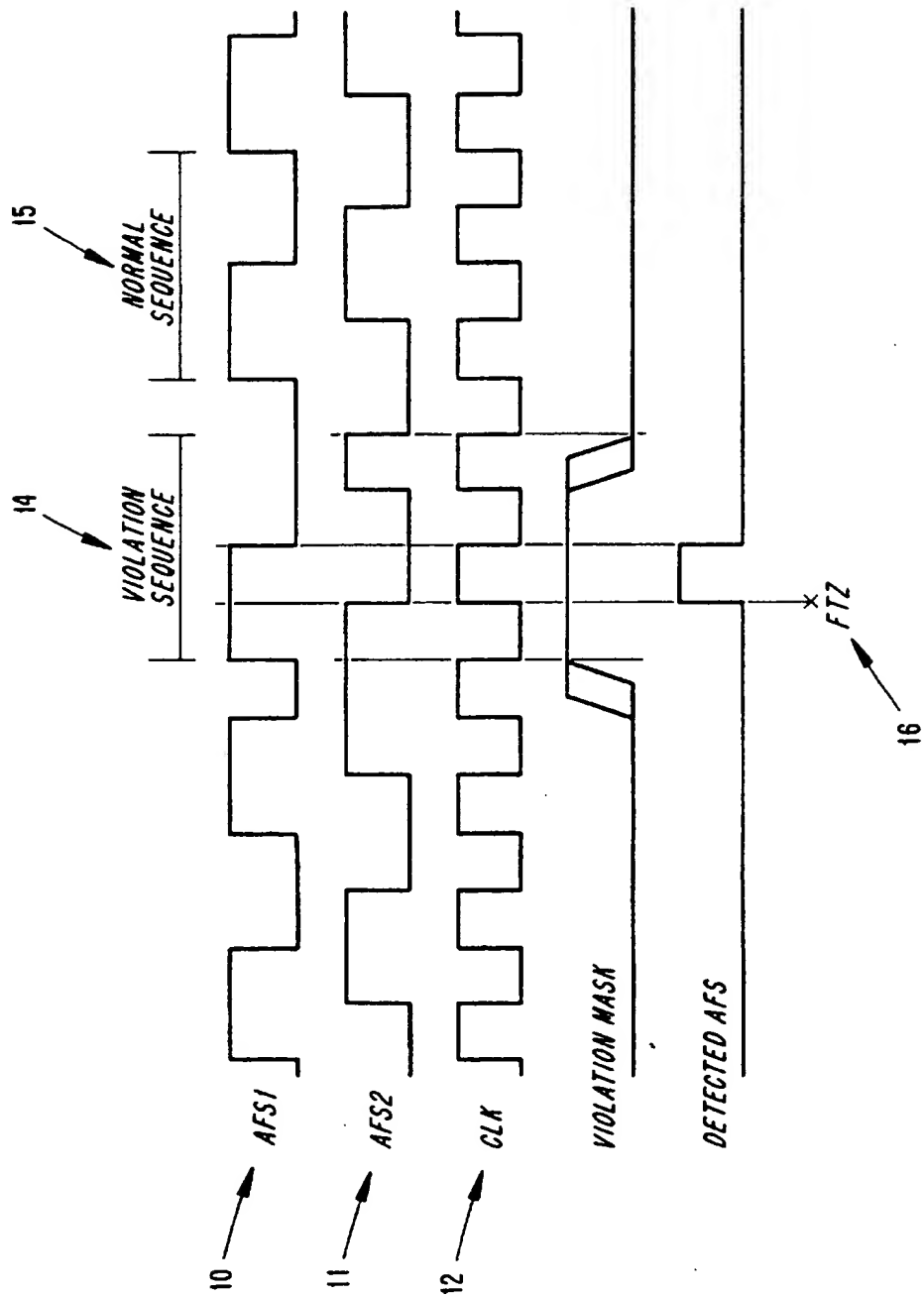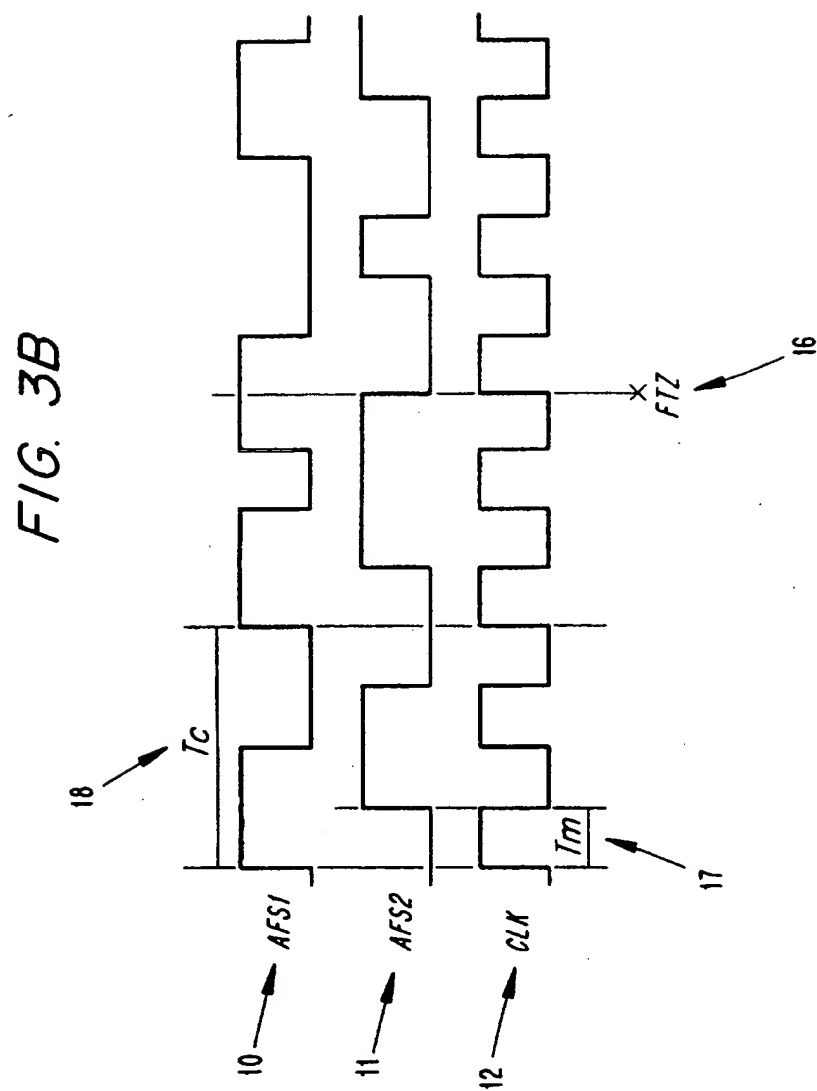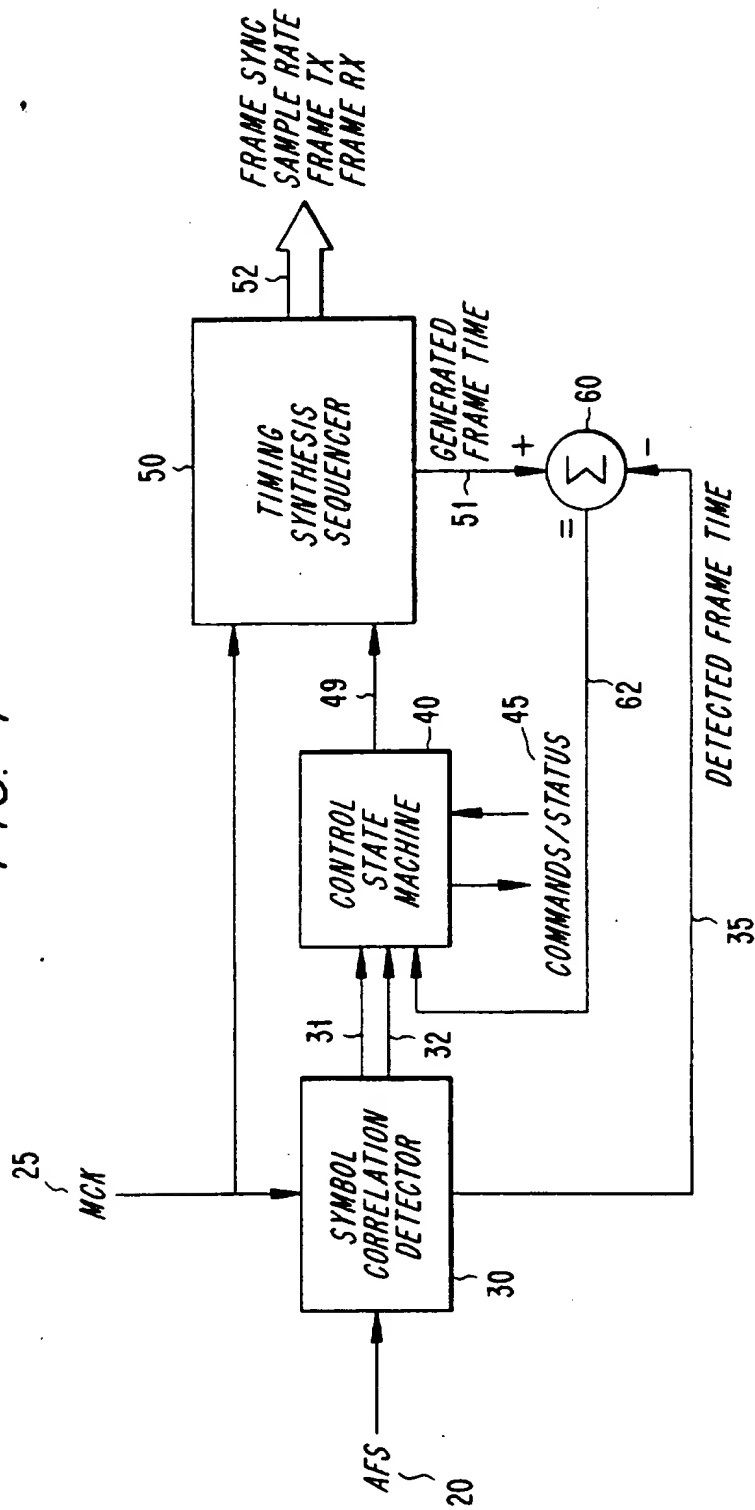
1/7

FIG. 1

ONE FRAME = 1944 BITS (972 SYMBOLS) = 40 MS. (25 FRAMES PER SECOND)

SLOT 1	SLOT 2	SLOT 3	SLOT 4	SLOT 5	SLOT 6

ONE SLOT

FIG. 2

BS1

TL1

MSC

MS

MS'

TL2

BS2

FIG. 3A

FIG. 3B

FIG. 4

FIG. 5

FIG. 6

FIG. 7

7/7
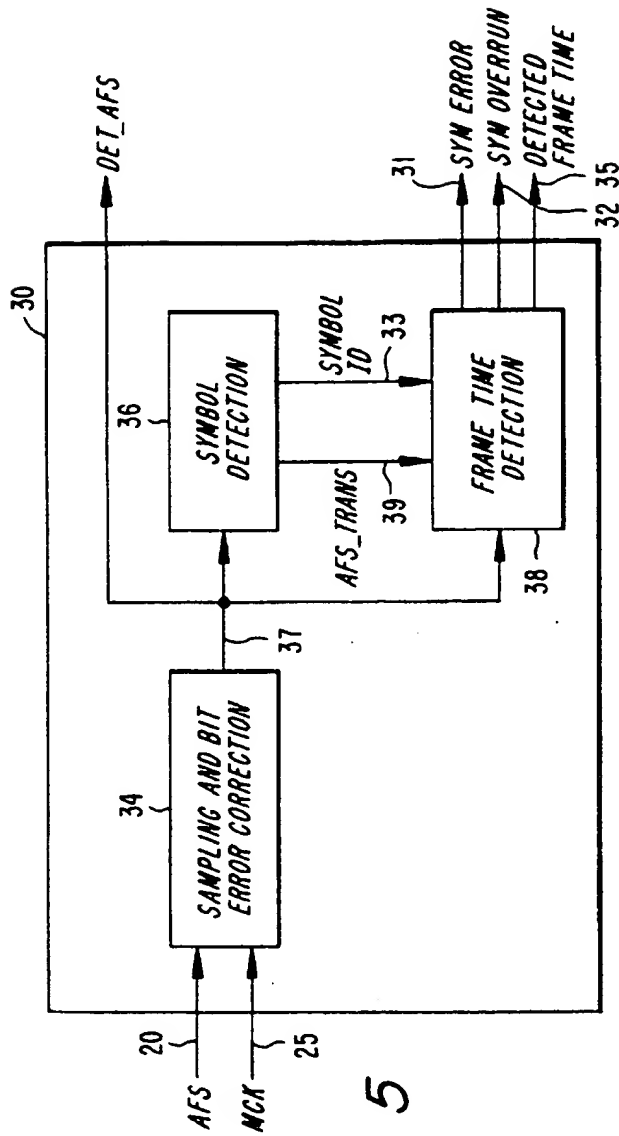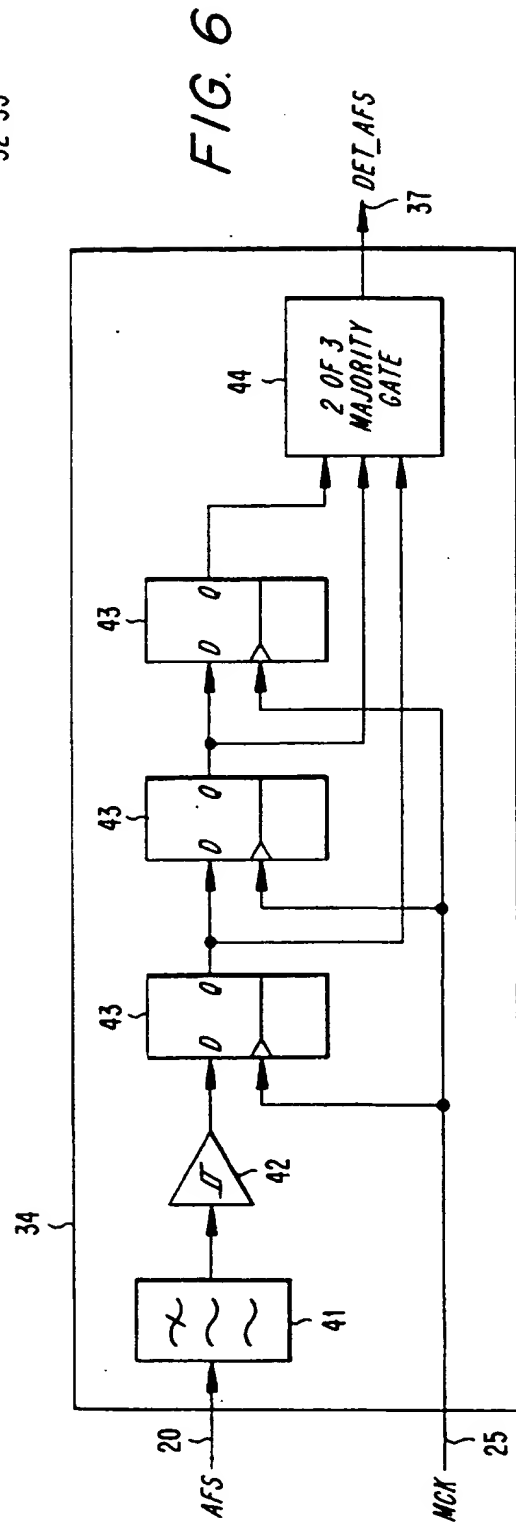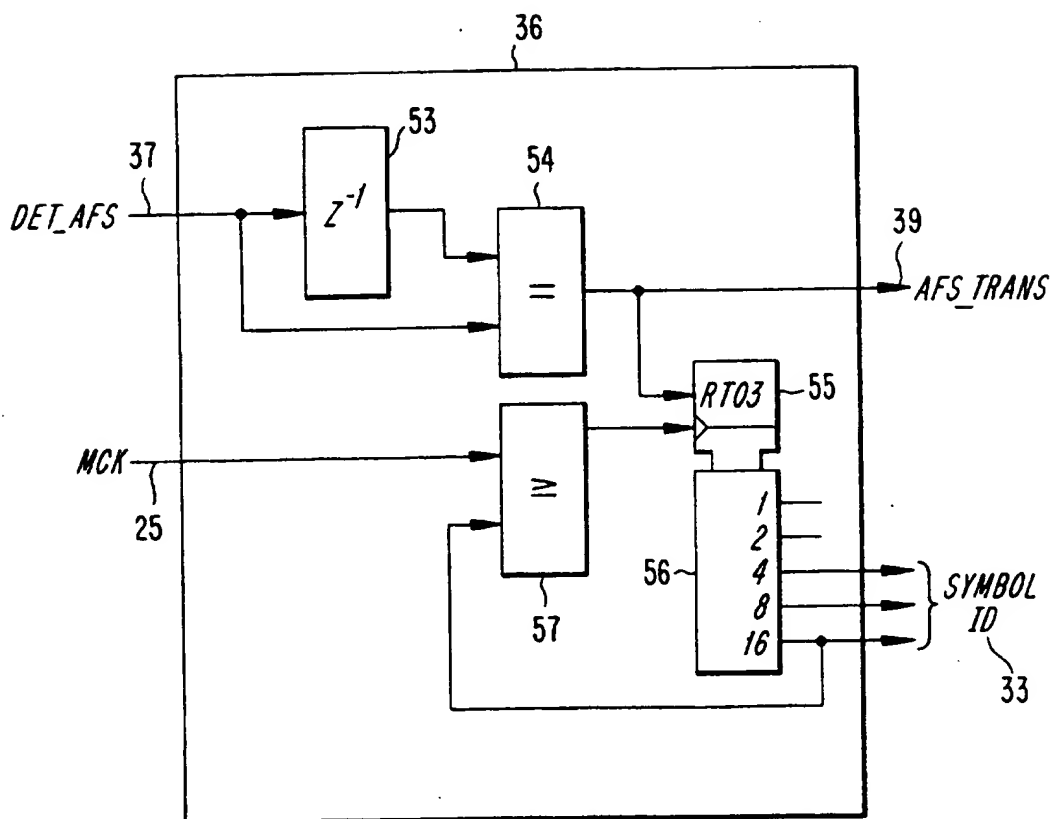
FIG. 8
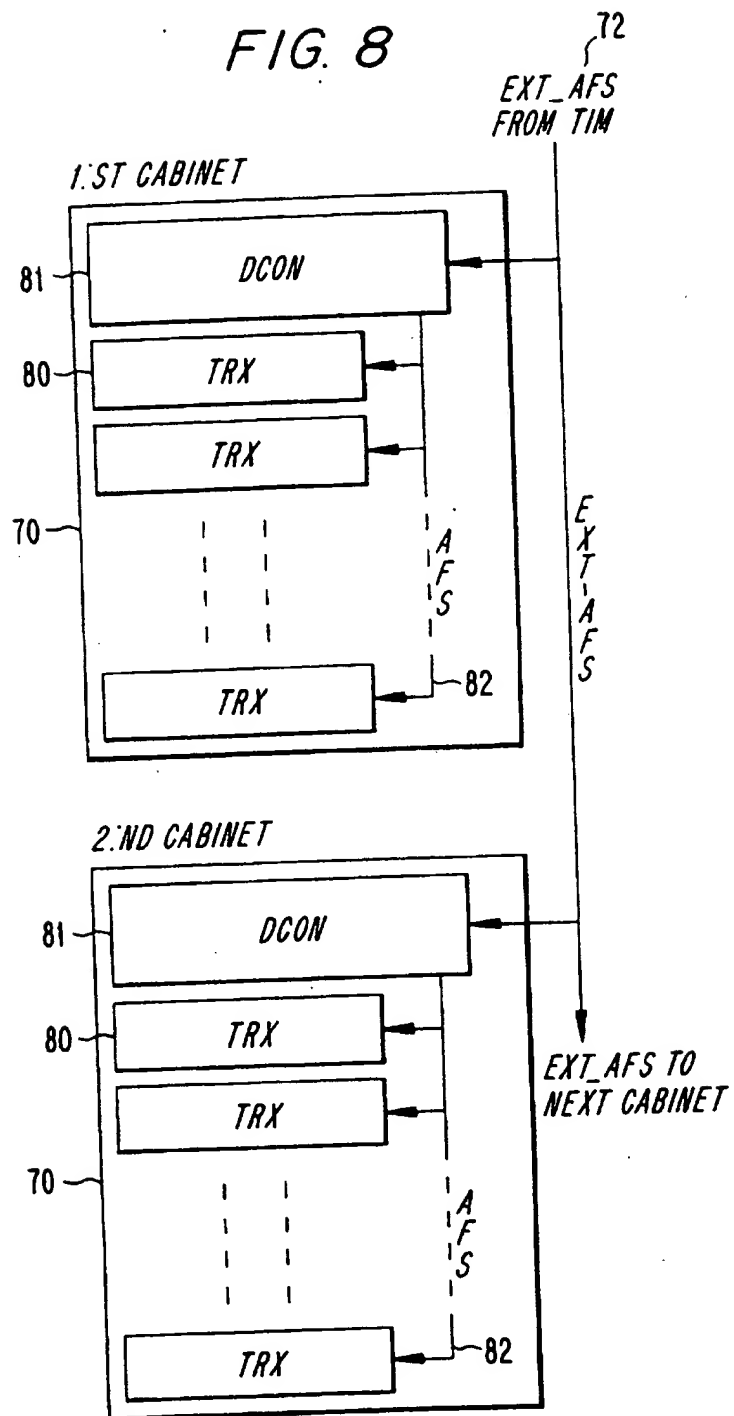
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PCT/US 96/19653

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H04J3/06   H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H04J   H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 218 770 A (WELLER DAVID R) 19 August 1980 see column 1, line 13 - line 28 see column 1, line 66 - column 2, line 17 see column 7, line 29 - line 49 ---	1-16,18, 19
X	US 4 683 567 A (GREEN MICHAEL J ET AL) 28 July 1987 see column 1, line 39 - column 2, line 8 see column 5, line 18 - column 6, line 8 ---	1,19
A	EP 0 553 610 A (SIEMENS AG) 4 August 1993 see page 2, line 30 - line 42 see page 2, line 53 - line 58 see page 4, line 1 - line 29 ---	1-19

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[X] Further documents are listed in the continuation of box C.   [X] Patent family members are listed in annex.

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Date of the actual completion of the international search

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 671 825 A (SEL ALCATEL AG) 13 September 1995 see column 3, line 26 - column 4, line 8 -----	1-19

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4218770 A	19-08-80	NONE	
US 4683567 A	28-07-87	CA 1234644 A	29-03-88
EP 0553610 A	04-08-93	DE 4202341 A	05-08-93
		CA 2088210 A	30-07-93
		JP 5276154 A	22-10-93
		JP 7022286 B	08-03-95
EP 0671825 A	13-09-95	DE 4407794 A	14-09-95
		CA 2143930 A	10-09-95